REMARKS

Claims 1-15, and 17-30 stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion. Claim 17 is objected to based on informalities and is amended herein to overcome the objection. Therefore, claims 11-12 are herein cancelled. Thus, claims 1-10, 13-15, and 17-30 are all the claims presently pending in the application.

I. The Prior Art Rejections

Claims 1-15 and 17-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Jacobson (U.S. Patent No. 7,073,110), hereinafter referred to as Jacobson, Nadeau-Dostie et al. (U.S. Patent No. 6,829,730), hereinafter referred to as Nadeau-Dostie. Applicants respectfully traverse these rejections based on the following discussion.

A. Summary of the Cited Prior Art References

1. Jacobson. Jacobson discloses a TAP controller which can be muxed to multiple embedded TAPS. The architecture a programmable instruction register and logic 304c for a flexible length instruction register so as to match the length of a particular one of the embedded TAPs. In the register and logic a plurality of serially arranged bit registers (376, 378, 380) can be connected in series with an existing fixed length instruction register 382. By selecting an outer one of the serially arranged bit registers, the length of the existing fixed length instruction register segment 382 can be extended (see Abstract, Figure 3c and col. 8, line 49- col. 9, line 51). Thus, as explained in col. 9, lines 11-30, each of the bit register segments 376, 378, 380 incrementally extend the length x of the fixed bit register segment 382 by one bit. For example, selection of bit register 376 will extend the length x of the fixed bit register 382 by 1 bit (providing a total length of x+1bit), selection of bit register 378 will extend the length x of the fixed bit register 382 by 2 bits (providing a total length of x+2bits) and so on until the selection of bit register 380 which will extend the length the fixed bit registers 380 by N bits (providing a total length of x+Nbits). To allow for selection of a particular bit register, each bit register is coupled to a corresponding selector which in turn is coupled to a programmable bit select

register. Each of the programmable bit select registers can be programmed to enable its corresponding selector to select its corresponding bit register.

2. Nadeau-Dostie. Nadeau-Dostie also teaches a circuit with a Master TAP (i.e., TAP controller) connected to multiple embedded TAPs. The embedded TAPs are arranged into one or more groups and the master TAP has a fixed length instruction register.

B. Summary of the Claimed Invention

As disclosed in paragraphs [0021-0023] and illustrated in Figure 1, in the present invention a chip-level TAP is connected to multiple embedded TAPs. The chip-level TAP comprises a chip-level instruction register that has a flexible length so as to match the length of a particular one of the embedded TAP instruction registers. The chip-level instruction register comprises a plurality of instruction register segments and additional bit segments. These instruction register segments comprise a first instruction register segment that has the same length (E.g., 4 bits) as the shortest embedded TAP instruction register and at least two other instruction register segments that have lengths equal to a difference between a previous shorter embedded TAP instruction register and a next longer embedded TAP instruction register (e.g., a second register segment that has a length equal to the difference between the shortest embedded TAP instruction register and a next longer embedded TAP instruction register).

The overall length of all of the instructions register segments is equal to the length of the longest instruction register amongst the embedded TAPs. Thus, the overall length of the chip-level instruction register is equal to the length of the longest embedded TAP instruction register plus the length of the additional bits. Consequently, with the additional bit segments the chip-level flexible length instruction register is longer than the longest embedded TAP instruction register. The additional bits in the chip-level instruction register are adapted to choose the effective length of the flexible length instruction register so that it will equal the combined length of the first instruction register segment and any selected other instruction register segments so as to match the length of a particular one of the embedded TAP instruction registers.

C. Rejection Of Amended Independent Claim 1 Based On Jacobson and Nadeau-

Dostie

The Applicants submit that neither of the cited prior art references teach or suggest the following feature of amended independent claim 1: "wherein at least two of said instruction register segments comprise multiple bits".

As discussed in the previously filed amendment dated October 23, 2006, only the fixed length bit register 382 of Jacobson with a length of x has multiple bits. The bit registers 376, 378, etc. each comprise single bits that are added incrementally to the fixed length bit register to increase its length by one additional bit (e.g., to provided combined lengths of x+1, x+2, etc.). Thus, as acknowledged by the Examiner, Jacobson does not teach a chip-level test access port (TAP) controller that has an instruction register that comprises a plurality of instruction register segments, wherein at least two of said instruction register segments comprise multiple bits.

Consequently, the most recent Office Action cites Nadeau-Dostie as teaching this feature. Specifically, the Office Action indicates that it "would have been obvious to one of ordinary skill ... to modify Jacobson's bit registers 376, 378, ... 380 to have multiple bits as in Nadeau-Dostie embedded TAPS 102, 104 and 106." The Applicant's respectfully disagree.

More specifically, per col. 2, lines 35-40 the Nadeau-Dotsie invention provides a single master TAP which functions as the bus for controlling data transfer operations with secondary TAPs in the circuit (e.g., like the chip-level TAP controller of the present invention). Fig. 3 is described in the text of Nadeau-Dotsie as illustrating a Master TAP 100 connected to three embedded secondary TAPs 102, 104 and 106. Each secondary TAP has its own instruction registers 116, 118 and 120, respectively, which each have three shift register elements. Multiple embedded TAPs can be serially connected in a group (e.g., group 114 can comprise two embedded TAPs, e.g., 104 and 106, including their respective instruction registers). However, the Master TAP is the sole member of its group. Per col. 10, lines 1-5, within each group all of the instruction registers are combined and the instruction register 125 of the Master TAP 100 should be made so that its length is equal to the length of the longest combined instruction register plus a selection code bit(s). That is, the Master TAP 100 (i.e., the TAP controller) will be made to have an instruction register with a fixed length and this predetermined fixed length will be equal to the combined length of multiple TAP instruction registers from a grouping of

embedded TAPs. Master TAP 100 of Nadeau-Dostie does not comprise an instruction register with at least two segments comprising multiple bits.

Therefore, there is no motivation or suggestion to modify Jacobson's bit registers 376, 378, ... 380 to have multiple bits as in Nadeau-Dostie embedded TAPS 102, 104 and 106 to support of an obviousness rejection (see MPEP §2143.02). More specifically, the fixed instruction register 125 of the Master TAP 100 (connected to multiple embedded TAPs 102, 104 and 106) in Figure 3 of Nadeau-Dostie correlates to the instruction register 304c (muxed to multiple embedded TAPs 318) of Figure 3c of Jacobson. However, Jacobson and Nadeau-Dostie each disclose different incompatible ways of determining the length of the primary TAP instruction register. In one the length is fixed, in the other it is flexible to accommodate different secondary instruction register lengths. Each of the embedded TAPs 102-106 of Nadeau-Dostie has an instruction register with multiple bits and several of the embedded TAPS 104-106 can be connected serially in a group. There is no motivation or suggestion to combine the grouping of the embedded TAPs of Nadeau-Dostie with the programmable instruction register and logic structure of Jacobson in order to make obvious a TAP controller that has a flexible length instruction register that comprises a plurality of instruction register segment having multiple bits. In fact Nadeau-Dostie teaches away from this by indicating that the Master TAP 100 must be a group of one (i.e., is not combined with other TAPs) (see col. 10, lines 54-56).

Therefore, amended independent claim 1 is patentable over a combination of Jacobson and Nadeau-Dotsie. Further, dependent claims 2-9 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

D. Rejection Of Amended Independent Claim 10 Based On Jacobson and Nadeau-Dostie

The Applicants further submit that neither of the cited prior art references teach or suggest the following features of amended independent claim 10: (1) "wherein said flexible length instruction register comprises a plurality of instruction register segments at least two of which comprise multiple bits; and additional bit segments"; (2) "wherein said plurality of instruction register segments comprise: a first instruction register segment having a same length as a shortest embedded TAP instruction register; and a second instruction register segment having a length equal to a difference between said shortest embedded TAP instruction register and a next longer embedded TAP instruction register"; (3) "wherein all of said instruction register segments combined are as long as a longest embedded TAP instruction register"; (4) "wherein said additional bit segments make said flexible length instruction register longer than said longest embedded TAP instruction register"; and (5) "wherein said additional bit segments comprise bits that are adapted to choose an effective length of said flexible length instruction register."

Regarding the feature of "wherein said flexible length instruction register comprises a plurality of instruction register segments at least two of which comprise multiple bits", see the detailed discussion regarding this same feature in Claim 1 above.

Regarding the features "wherein said plurality of instruction register segments comprise: a first instruction register segment having a same length as a shortest embedded TAP instruction register; and a second instruction register segment having a length equal to a difference between said shortest embedded TAP instruction register and a next longer embedded TAP instruction register" and "wherein all of said instruction register segments combined are as long as a longest embedded TAP instruction register", the Office Action again cites a Jacobson- Nadeau-Dostie combination. Specifically, the Office action refers to the Jacobson bit registers 376, 378, ...380, Fig. 3C of Jacobson and the embedded TAPs of Nadeau-Dostie col. 3, lines 10-14, 38-41 and col. 7, lines 36-41. The Applicants again respectfully disagree for the same reasons as discussed above with regard the feature of "wherein said flexible length instruction register comprises a plurality of instruction register segments at least two of which comprise multiple bits."

Additionally, the fixed length bit register 382 of Jacobson has a length of x has multiple bits. Nowhere in Jacobson is it disclosed that this length x is a same length as that of the shortest

embedded TAP instruction register. In fact the determining factor for the length of the fixed segment 382 is not disclosed in Jacobson. Furthermore, the bit registers 376, 378, etc. each comprise single bits that are added incrementally to the fixed length bit register to increase its length by one additional bit (e.g., to provided combined lengths of x+1, x+2, etc.). Therefore, nowhere in Jacobson does it disclose that a second instruction register segment (e.g., 376) has a length equal to the difference between the length of the shortest embedded TAP instruction register and a next longer embedded TAP instruction register." That is, Jacobson does not teach a plurality of instruction register segments of which at least two comprise multiple bits, nor does it teach what the lengths of those segments correspond to (other than 1).

In Nadeau-Dostie, the instruction register of the Master TAP is not segmented or flexible and the length of the instruction register 125 of the Master TAP is fixed.

Regarding the features of "wherein said flexible length instruction register comprises ... additional bit segments", "wherein said additional bit segments make said flexible length instruction register longer than said longest embedded TAP instruction register" and "wherein said additional bit segments comprise bits that are adapted to choose an effective length of said flexible length instruction register", the Office Action provides that "Jacobson in view of Nadeau-Dostie teaches the flexible length instruction register further comprises additional bit segments all of said instruction register segments combined are as long as said longest embedded TAP instruction register comprises bits that are adapted to choose the active segments of said flexible length instruction (bit registers 376, 378, ... 380 coupled to selector 370, 372 ... 374 respectively, Fig. 3c). (Jacobson, col. 8, l. 49 to col. 9, l. 51.) (Nadeau-Dostie, Fig. 3, col. 3, ll. 10-14, 38-41, col. 7, ll. 36-41, col. 9, l. 47 to col. 10, l. 17)". The Applicants respectfully disagree.

Per paragraph [0022], the specification of the claimed invention provides that the flexible instruction register of the TAP controller comprises instruction register segments as well as additional bits. The additional bits are adapted to choose the effective length of the flexible length register. Specifically, a selection logic 130 uses information contained in the additional bits (not contained in the instruction register segments) to identify which register segments will be used in the flexible length instruction register.

Contrarily, in Jacobson separate selectors 370, etc. are connected to each and every single-bit instruction register segment that can be added to the fixed register. A programmable bit select register is programmed to enable a selector corresponding to a given bit which in turn selects its corresponding bit register (see col. 9, lines 11-51). For example, bit select register 368 can be programmed to enable selector 374 and thereby to select outer bit register 380. Selection of a specific bit results in the selection of all bit registers from the fixed bit register 382 to the outer bit register 380. Therefore, Jacobson does not disclose that any additional bits in its programmable bit register are actually adapted to choose an effective length.

Furthermore, Nadeau-Dotsie teaches that its fixed length instruction register includes a predetermined number of additional bits; however, per col. 3, lines 1-10, these additional bits are for storing a TAP selection code for selecting one of the TAPs. A TDO circuit responds to this TAP selection code and selectively connects the TDO of one of the embedded TAPs to the circuit TDO. Nowhere in Nadeau-Dotise does it teach or suggest that the additional bits are not adapted to choose an effective length of the instruction register itself.

Therefore, amended independent claim 10 is patentable over a combination of Jacobson and Nadeau-Dotsie. Further, dependent claims 13-14 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

E. Rejection Of Amended Independent Claim 15 Based On Jacobson and Nadeau-Dostie

The Applicants submit that Jacobson does not teach or suggest the following features of amended independent claim 15: (1) "wherein said flexible length instruction register comprises a plurality of instruction register segments having a combined length equal to a longest embedded TAP instruction register and additional bit segments such that said flexible length instruction

register is longer than said longest embedded TAP instruction register"; (2) "wherein said plurality of instruction register segments comprise: a first instruction register segment comprising multiple bits and having a same length as a shortest embedded TAP instruction register; and at least two other instruction register segments having lengths equal to a difference between a previous shorter embedded TAP instruction register and a next-longer embedded TAP instruction register" and (3) "wherein at least one of said at least two other instruction register segments comprises multiple bits." See the discussion above regarding the same or similar features in claims 1 and 10.

Therefore, amended independent claim 15 is patentable over a combination of Jacobson and Nadeau-Dotsie. Further, dependent claims 17-21 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

F. Rejection Of Amended Independent Claim 22 Based On Jacobson and Nadeau-Dostie

The Applicants submit that Jacobson does not teach or suggest the following features of amended independent claim 22: (1) "wherein said flexible length instruction register comprises a plurality of instruction register segments having a combined length equal to a longest embedded TAP instruction register and additional bit segments such that said flexible length instruction register is longer than the longest embedded TAP instruction register"; and (2) "wherein said additional bit segments are adapted to choose an effective length of said flexible length instruction register." See the discussion above regarding the same or similar features in claims 1, 10 and 15.

Therefore, amended independent claim 22 is patentable over a combination of Jacobson and Nadeau-Dotsie. Further, dependent claims 23-30 are similarly patentable, not only by virtue

of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

III. Formal Matters and Conclusion

With respect to the claim rejections, the claims have been amended, above, to overcome these rejections. With respect to the objection to claim 17, claim 17 has also been amended to overcome this objection. In view of the foregoing, Applicants submit that claims 1-10, 13-15 and 17-30, all the claims presently pending in the application, are patentably distinct from the prior art of record and are now in condition for allowance. Therefore, the Examiner is respectfully requested to reconsider and withdraw the rejections of all pending claims and the objection to claim 17. The Examiner is also respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: March 15, 2007

/Pamela M. Riley/
Pamela M. Riley
Registration No. 40,146

Gibb & Rahman, LLC
2568-A Riva Road, Suite 304
Annapolis, MD 21401
Voice: (410) 573-1528
Fax: (301) 261-8825
Customer Number: 29154